

REMARKS

After entry of this amendment, claims 1-31 remain pending. In the present Office Action, claims 19-31 were rejected under 35 U.S.C. § 112, second paragraph. Claims 19, 21-24, 26-28, and 30-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Stallings, "Computer Organization and Architecture", 1996 ("Stallings"). Applicant respectfully traverses this rejection and requests reconsideration. Claims 20, 25, and 29 were objected to as being dependent from a rejected base claim but would be allowable if rewritten in independent form. Claims 1-18 are allowed.

Section 102 Rejection

Applicant respectfully submits that each of claims 19-31 recite combinations of features not taught or suggested in the cited art. For example, claim 19 recites a combination of features including: "the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by a processor even if an instruction specifying the corresponding segment register is executed by the processor".

The Office Action alleges that the above highlighted features are taught by certain addressing modes described by Stallings. Particularly, the Office Action refers to both the displacement addressing mode and the immediate or register addressing modes to allegedly anticipate the first protected operating mode. However, a given instruction encoding can specify only ONE addressing mode. Furthermore, each of Stallings' addressing modes either: (i) specify a segment register and the contents thereof are used by the processor during execution of the instruction; or (ii) do not specify a segment register. For example, the immediate addressing mode and the register addressing mode each do not specify a segment register, as indicated in table 10.2. Accordingly, instructions having the immediate or register operand modes do not specify a segment register and thus fail to anticipate "the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by a processor even if an instruction specifying the corresponding segment register is executed by the processor" as recited in claim 19. With regard to the register addressing

mode, Stallings also teaches that some instructions reference the segment registers (Stallings, page 370, second paragraph, last sentence). However, these instructions then use the contents of the segment register during execution. Accordingly, these teachings also fail to teach or suggest the above highlighted features. The remaining addressing modes specify a segment register, and the segment register contents are used during execution of the instruction. For example, Stallings teaches "The remaining addressing modes reference locations in memory. The memory location must be specified in terms of the segment containing the location" (Stallings, page 370, third paragraph). Again, since these addressing modes specify a segment register and the contents thereof are used during execution, these addressing modes fail to teach or suggest "the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by a processor even if an instruction specifying the corresponding segment register is executed by the processor" as recited in claim 19.

With regard to the immediate or register addressing modes, the Office Action notes that "in such as immediate mode or register mode, SR is not used even though the segment descriptors are stored in the system" (see, e.g., Office Action, page 4, lines 1-3). While this statement may be true, this still does not teach or suggest "the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by a processor even if an instruction specifying the corresponding segment register is executed by the processor" since the immediate and register addressing modes do not specify a segment register.

Additionally, the Office Action alleges that the addressing modes are best reasonably and broadly interpreted as the addressing modes since the protected operating mode is not well described in claim 19 (see, e.g., Office Action, page 4, lines 9-11). Applicant respectfully submits that Stallings addressing modes do not teach or suggest the combination of features recited in claim 19, as highlighted above. Furthermore, Applicant respectfully submits that the term "protected mode" has a well understood meaning in the art that does not require definition in the claim. For example, see the specification, page 11, lines 5-7.

For at least the above stated reasons, Applicant submits that claim 19 is patentable over the cited art. Claims 20-23 depend from claim 19 and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 20-23 recites additional combinations of features not taught or suggested in the cited art.

Claim 24 recites a combination of features including: "the execution core is configured to load one or more segment descriptors into one or more of the plurality of segment registers responsive to one or more segment load instructions, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by the execution core even if a first instruction specifying the corresponding segment register is executed by the execution core". The teachings of Stallings, highlighted above, do not teach or suggest the above highlighted combination of features either. Accordingly, Applicant submits that claim 24 is patentable over the cited art. Claims 25-27 depend from claim 24 and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 25-27 recites additional combinations of features not taught or suggested in the cited art.

Claim 28 recites a combination of features including: "the processor is configured to load one or more segment descriptors into one or more of the plurality of segment registers responsive to one or more segment load instructions, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used by the processor even if a first instruction specifying the corresponding segment register is executed by the processor". The teachings of Stallings, highlighted above, do not teach or suggest the above highlighted combination of features either. Accordingly, Applicant submits that claim 28 is patentable over the cited art. Claims 29-31 depend from claim 28 and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 29-31 recites additional combinations of features not taught or suggested in the cited art.

Section 112 Rejection

The Office Action asserts that the phrase "at least one of the one or more segment descriptors is not used" is unclear since the device that does not use the segment descriptors is not stated. Applicant respectfully disagrees with the rejection and submits that the phrase is clear in context of the claim. However, Applicant has amended claims 19 and 28 to recite "at least one of the one or more segment descriptors is not used by the processor" and has amended claim 24 to recite "at least one of the one or more segment descriptors is not used by the execution core". Applicant submits that the amendment addresses the section 112 rejection.

CONCLUSION


Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-65900/LJM.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Request for Approval of Drawing Changes
- ☐ Notice of Change of Address
- ☐ Please debit the above deposit account in the amount of \$ for fees ().
- ☐ Other:

Respectfully submitted,



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